REMARKS

Applicant appreciates the thorough examination of the present application that is reflected in the Official Action of January 16, 2003. However, notwithstanding this thorough examination, Applicant respectfully submits that original Claims 1-20 are patentable for the reasons that will be described in detail below. Moreover, new Claims 21-31 also are patentable for the reasons that will be described in detail below. For the convenience of the Examiner, the reasons for patentability will be analyzed in the order in which the rejections were presented in the Detailed Action of January 16, 2003.

Claim 1 Is Patentable Over U.S. Patent 5,663,596 to Little

Claim 1 was rejected under 35 USC §102(b) as being anticipated by Little. However, Applicant respectfully submits that Claim 1 recites:

> 1. A microelectromechanical (MEM) module comprising:
> a plurality of MEM device substrates, each of which includes at least one MEM device thereon;
> a base substrate including a face; and
> a mounting structure that is configured to mount the plurality of MEM device substrates on the face. (Emphasis added.)

Applicant respectfully submits that the passage of Little cited by the rejection confirms the lack of teaching or suggestion in Little of the above emphasized recitations of Claim 1. In particular, Little Column 6, lines 18-24 states:

> Consequently, they are usually combined on a substrate as exemplified by FIG. 7. With the teachings of the present invention, an MEM chip **112** and an associated electronics chip **102** could be combined as shown in FIGS. 6A and 6B in which the spring contacts **104** have already been fabricated at the wafer level of the chip **102**. (Emphasis added.)

Thus, this passage clearly teaches that a single MEM chip and a single electronics chip are combined on the substrate. In contrast, Claim 1 recites a plurality of MEM device substrates which are mounted on a base substrate. Moreover, it would not be obvious to modify Little to provide a plurality of MEM device substrates, because Little specifically teaches the advisability of combining a single MEM substrate and a single electronic circuit chip. See, for example, Little Column 6, lines 3-18:

> The present invention is particularly suited for situations in which an electronic system must be partitioned among a plurality of integrated circuits which are then mounted on a common substrate. For example, many systems

> (e.g., an accelerometer-based, control-loop system) include micro-machined modules (MEMs) and associated electronic circuits. MEMs typically share many of the basic processes, e.g., photolithographic pattern definition, masking and etching, that are conventionally used in electronic chips. However, the processes have differences (e.g., the degree of etching in an MEM is typically deeper and more extensive than the same process in an electronic chip), which generally cause MEMs and their associated electronics to be fabricated on separate wafers.

Accordingly, it would not be obvious to modify Little to provide a plurality of MEM device substrates on a base substrate, as recited in Claim 1.

Claims 2-5 Are Patentable Over Little in View of U.S. Patent 6,005,649 to Krusius et al.

Dependent Claims 2-5 are patentable at least per the patentability of independent Claim 1 from which they depend. Moreover, at least some of these claims are independently patentable.

For example, Claim 2 recites:

> 2. A MEM module according to Claim 1 wherein each of the MEM device substrates includes an array of M rows and N columns of MEM devices thereon and wherein the mounting structure is configured to mount the plurality of MEM device substrates in an array of R rows and S columns on the face to thereby provide a tiled array of M x R rows and N x S columns of the MEM devices in the MEM module.

The rejection concedes that Little fails to teach any of the recitations of Claim 2. However, the rejection cites Krusius et al. as teaching "each of the MEM device substrates includes an array of M rows and N columns of MEM devices thereon", as noted in the Detailed Action Page 3.

However, Applicant respectfully submits that, to establish a *prima facie* case of obviousness, three basic criteria must be met. The prior art reference (or references when combined) must teach or suggest *all* the claim limitations. There must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings, and there must be a reasonable expectation of success of the combination. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found *in the prior art*, not in applicant's disclosure. See MPEP § 2143. As recently affirmed by the Court of

Appeals for the Federal Circuit, to support combining references in a § 103 rejection, evidence of a suggestion, teaching, or motivation to combine must be *clear and particular*, and this requirement is not met by merely offering broad, conclusory statements about teachings of references. *In re Dembiczak*, 50 USPQ2.d 1614, 1617 (Fed. Cir. 1999).

Applicant respectfully submits that it would not be obvious to substitute Krusius et al.'s tiled flat-panel microdisplay array having visually imperceptible seams (as noted in the Krusius et al. title) into Little, for at least two reasons. First, as understood by Applicant, Little teaches away from the use of multiple MEM device substrates as was described above in connection with Claim 1. Moreover, as understood by Applicant, since Little combines an integrated circuit chip and a MEM chip, this combination would not produce any kind of tiling effect, whereas Krusius et al. combines microdisplay arrays to provide visually imperceptible seams. Finally, the rationale provided by the Detailed Action at the middle of Page 3, "to provide a compact, lightweight and inexpensive modules" represents a broad, conclusory statement that is impermissible under the case law and the MPEP. For at least these reasons, Claim 2 is independently patentable. Dependent Claims 3-5 are patentable at least per the patentability of Claim 2 from which they depend.

Claims 6-8 and 11 Are Patentable Over Krusius et al. In View of U.S. Patent 6,108,118 to Minamoto and In Further View of U.S. Patent 6,275,326 to Bhalla et al.

Claim 6 recites:

> 6. A microelectromechanical (MEM) mirror module comprising:
> a plurality of MEM mirror substrates, each of which includes a mirror comprising monocrystalline silicon, a frame comprising monocrystalline silicon that is spaced apart from and at least partially surrounds the mirror and at least two hinges between the mirror and the frame;
> a base substrate including a face; and
> a mounting structure that is configured to mount the frames of the plurality of MEM device substrates on the face.

At the top of Page 4 of the Detailed Action, the Detailed Action concedes that Krusius et al. teaches none of these recitations other than "A microelectromechanical (MEM) mirror module comprising: a plurality of MEM mirror substrates...". The Detailed Action relies on Minamoto's "optical deflector" (as noted in Minamoto's

title) in combination with the Bhalla et al. "control arrangement for microelectromechanical devices and systems" (as noted in Bhalla et al.'s title) to supply all of the missing teachings. In describing the motivation to combine these diverse references, the Detailed Action states, at the bottom of Page 4:

> Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Krusius et al., Minamoto and Bhalla et al. in order to provide an array of movable mirrors made of silicon for stiffness with a plurality of hinges for movability.

Applicant respectfully submits that this is the type of broad, conclusory statement that is not permitted by the case law or the MPEP.

Moreover, even if combined, the combination would not describe or suggest the recitations of Claim 6. In particular, the Detailed Action contends that Minamoto's mirror surface **106** corresponds to the claimed mirror comprising monocrystalline silicon, Minamoto's elastic member **152** corresponds to the claimed hinge, Minamoto's movable plate **101** corresponds to the base substrate, and Minamoto's support **103** corresponds to the claimed mounting structure. If this is the case, Minamoto clearly does not describe or suggest the claimed "frame comprising monocrystalline silicon that is spaced apart from and at least partially surrounds the mirror". Alternatively, if Minamoto's support **103** of Figure 2B corresponds to the claimed frame, then Minamoto does not describe or suggest the claimed "mounting structure that is configured to mount the frames of the plurality of MEM substrate devices on the face". Finally, if Minamoto's movable plate **101** corresponds to the claimed base substrate, then the support **103** of Minamoto et al. is not configured to mount the frame on the base, as recited in Claim 6. Accordingly, as Applicant understands it, there does not appear to be an interpretation of Minamoto Figure 2B that includes the claimed mirror, frame, hinge, base substrate and mounting structure in the relationship that is recited in Claim 6.

For purposes of this analysis, Applicant concedes that Bhalla et al. describes at least two hinges between a mirror and a frame. However, as was described above, it would not be obvious to combine the diverse teachings of Krusius et al in view of Minamoto in further view of Bhalla et al. and, even if combined, the recitations of Claim 6 would not be described or suggested.

Claims 7-8 and 11 are patentable as depending from patentable Claim 6. Moreover, Claims 7-8 and 11 are independently patentable for the reasons that will now be described.

In particular, Claim 7 recites:

> 7. A MEM mirror module according to Claim 6 wherein the frame is a first frame, each of the MEM mirror substrates also comprising an insulator layer on the first frame, opposite the mounting structure, and a second frame that is thicker than the first frame, on the insulator layer opposite the first frame.

The Detailed Action contends that in Minamoto Figure 5B, the first frame corresponds to movable plate **101**, the insulator layer corresponds to insulating film **102**, and the second frame corresponds to permanent magnet **108** and the Hall element wiring **109**. In this regard, Applicant respectfully submits that the Hall element **108** and the Hall element wiring **109** may not be regarded as a frame because the Hall element **108** and the wiring **109**, even if integrally formed, do not form a frame. Rather, the Hall element **108** operates as a sensor of movement as noted in Minamoto Column 4, line 45-Column 5, line 6, and the wiring conducts signals to and from the Hall element. Moreover, even assuming that elements **108** and **109** may be regarded as a frame, the movable plate **101** is much thicker than the Hall element **108** or the Hall element wiring **109**, as clearly shown in Minamoto Figure 5B, which is the opposite of that claimed. Accordingly, Claim 7 is independently patentable.

Claim 8 recites:

> 8. A MEM mirror module according to Claim 6 wherein the mirror includes a pair of opposing faces and wherein each of the MEM mirror substrates further comprises a metal layer on each of the opposing faces of the mirrors.

In this regard, the Official Action cites Minamoto Column 5, lines 42-45. However, this passage states:

> If the movable plate **101** is an Si substrate, then the mirror **106** may be formed of the polished surface of the substrate or a thin coating of aluminum or gold formed on the substrate.

This passage clearly shows that only one metal layer is formed on the movable plate **101**, as clearly illustrated in Minamoto Figure 2B. The other passage of Minamoto, at Column 8, lines 5-10, states:

> The structure shown in FIGS. 5A and 5B is characterized in that only one side of the movable plate has to be polished. This structure is advantageous in that the movable plate can be made of a low-priced material. In this connection, it should be noted that the structure shown in FIGS. 2A and 2B has to employ a movable plate both sides of which are polished.

This passage clearly shows that both sides of the movable plate **101** can be polished, but does not describe any technique for forming a metal layer on each side of the movable plate **101**. Accordingly, the recitations of Claim 8 are not described or suggested.

Finally, Claim 11 also is independently patentable. Claim 11 recites:

> 11. A MEM mirror module according to Claim 6 wherein each of the MEM mirror substrates includes an array of M rows and N columns of MEM mirrors thereon and wherein the mounting structure is configured to mount the plurality of MEM mirror substrates in an array of R rows and S columns on the face to thereby provide a tiled array of M x R rows and N x S columns of the MEM mirrors in the MEM mirror module.

The Official Action claims that Minamoto Column 4, lines 53-58 describes these recitations. However, this passage merely states:

> As shown in FIG. 1, when a current I is applied to a rectangular, thin semiconductor plate **50** and a magnetic flux density B is imposed in a direction (Z-direction) perpendicular to the current I, a Lorentz force is produced by interaction between the current I and the magnetic flux density B in a direction (Y-direction) orthogonal to both the X-direction and the Z-direction.

This passage clearly does not describe these recitations but, rather, describes how a Hall element works. Accordingly, Claim 11 is independently patentable.

Claims 12-15 and 17-20 Are Patentable Over Krusius et al. In View of Minamoto

Claim 12 recites:

> 12. A method of fabricating a microelectromechanical (MEM) mirror module comprising:
>
> providing a silicon-on-insulator substrate that includes a monocrystalline silicon layer on a bulk silicon substrate, with an insulator layer therebetween;
>
> fabricating at least two spaced apart pads in the monocrystalline silicon layer that extend through the monocrystalline silicon layer to the insulator layer;
>
> fabricating at least one hinge on each of the at least two spaced apart pads;

> defining a mirror and a frame that at least partially surrounds the mirror, in the monocrystalline silicon layer, such that the hinges bridge the mirror and the frame; and
>
> forming a metal layer on at least a portion of the mirror and at least a portion of the frame, opposite the insulator layer.

The Detailed Action concedes at Page 5 that Krusius et al. teaches a MEM module, but fails to teach any of the recitations of method Claim 12. In order to supply the many missing teachings, the Detailed Action cites Minamoto.

As an initial matter, Applicant respectfully submits that it would not be obvious to combine Krusius et al. with Minamoto for the reasons that were already described. Moreover, the rationale provided for the combination at Page 6 of the Detailed Action:

> Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Krusius et al. with Minamoto to provide a method of fabricating a tiled array of MEM devices,

is the type of broad, conclusory statement that is not permitted by the case law or the MPEP.

Moreover, even if combined, many of the recitations of Claim 12 would not be described or suggested. In particular, the Detailed Action states at Page 6 that the claimed insulator layer is shown in Minamoto as insulating film **110** of Figure 2B. However, even assuming that the movable plate **101** is monocrystalline silicon, the Hall element **108** on the opposite side of the insulating film **110** is not monocrystalline silicon. See, for example, Minamoto Column 6, lines 19-21:

> The Hall element **108** is preferably made of a material, such as InSb, InAs, GaAs, or the like, that has a large carrier mobility.

Accordingly, the claimed "monocrystalline silicon layer on a bulk silicon substrate, with an insulator layer therebetween" is not described or suggested.

Finally, the Detailed Action does not provide any citation to any teaching in Minamoto that describes the step of:

> fabricating at least two spaced apart pads in the monocrystalline silicon layer that extend through the monocrystalline silicon layer to the insulator layer...,

as recited in Claim 12. Also, although the Detailed Action states that the elastic member **152** of Minamoto corresponds to the claimed hinge, the Detailed Action does not point to any description or suggestion in Minamoto that describes:

fabricating at least one hinge on each of the at least two spaced apart pads..., as recited in Claim 12. Finally, assuming that in Minamoto Figure 2 the mirror corresponds to element **106** and the frame corresponds to element **103**, there is no description or suggestion of the claimed:

> forming a metal layer on at least a portion of the mirror and at least a portion of the frame, opposite the insulator layer.

Applicant also wishes to note that the embodiment of Figure 14B of Minamoto employs a silicon-on-insulator substrate, wherein a movable silicon substrate **301** and a movable plate Si include a movable plate SiO_2 therebetween. However, even in this figure, there is no description of fabricating pads, a hinge on the pads, a mirror, a frame and a metal layer, as recited in Claim 12. For at least these reasons, Claim 12 is patentable over Krusius et al. in view of Minamoto.

Claims 13-15 are patentable at least per the patentability of Claim 12 from which they depend. Moreover, Claims 13-14 are independently patentable. In particular, Claim 13 recites:

> 13. A method according to Claim 12 further comprising:
> etching the bulk silicon substrate to expose the insulator layer adjacent the mirror and adjacent the pads; and
> etching the insulator layer adjacent the mirror and the pads to release the mirror and the hinges.

The Detailed Action cites Minamoto Figure 5A, Column 7, lines 49-67 and Column 8, lines 1-11. However, in Minamoto Figure 5A, there do not appear to be any pads at all, so that there does not appear to be any etching of the bulk silicon substrate to expose the insulating layer and there does not appear to be any etching of the insulating layer to release the mirror and the hinges. To the contrary, the passages cited by the Official Action describe how to form a mirror surface by removing the insulating film **102** and coating a metallic film thereon. Etching of the bulk silicon substrate is not described or suggested. The Detailed Action states, at the very last sentence of Page 6, that:

> It is a fundamental design choice to etch the insulator layer adjacent the mirror and the pads to release the mirror and the hinges.

However, Applicant respectfully submits that it is not a fundamental design choice based on the teachings of Minamoto, because Minamoto does not describe pads, does not describe any etching of the bulk silicon substrate, and does not describe releasing the mirror or the hinges. Accordingly, Claim 13 is independently patentable.

Claim 14 recites "forming a second metal layer on the mirror opposite the first metal layer". The Detailed Action contends at the top of Page 7 that:

> The office interprets the first metal layer to form the driving coil 104 (col. 7, ln. 13-16), which is opposite the mirror 106.

Assuming for the sake of argument that the driving coil **104** is the first metal layer, there is no second metal layer, and if mirror surface **106** is determined to be a second metal layer, it is not on the mirror **101** opposite the first metal layer but, rather, is on the same side as the first metal layer. For at least these reasons, Claim 14 is independently patentable.

Finally, Claim 17 recites:

> 17. A method of fabricating a movable microelectromechanical (MEM) structure comprising:
> etching an array of features in a silicon substrate;
> at least partially thermally oxidizing the array of features to form a pad comprising silicon dioxide in the silicon substrate;
> forming a movable MEM structure on the pad; and
> removing the pad to release the movable MEM structure.

The Detailed Action cites to Minamoto Figure 14B. However, the Detailed Action does not describe any recitation in Minamoto that describes the claimed "etching an array of features in a silicon substrate". There is no such array of features in Figure 14B. Moreover, the Detailed Action does not cite to any description in Minamoto of the claimed "at least partially thermally oxidizing the array of features to form a pad comprising silicon dioxide in the silicon substrate". There does not appear to be any description of thermally oxidizing an array of features or any pad shown in Figure 14B. Also, the only conceivable movable MEM structure in Minamoto Figure 14B appears to be the movable plate SiO_2 or the movable plate Si, and these are not shown as being formed on any kind of pad. Rather, they are formed directly on the substrate **301**. Finally, there is no description or suggestion of removing a pad, because there is no pad in Minamoto Figure 14B.

In rejecting Claim 17, the Detailed Action cites to Minamoto Column 7, lines 1-20. This passage recites:

> Hereinafter, an example of a method of manufacturing the optical deflector using an Si substrate as the movable plate **101** will be described briefly. First, an insulating film, serving as a mask for subsequent etching of Si, is formed on one surface of an Si substrate by means of sputtering, CVD, vacuum evaporation, or the like and then patterned using photolithographic techniques. Next, an organic insulating film **102** is formed on the opposite surface of the Si substrate by means of spin coating, screen printing, or the like and then patterned. This organic insulating film **102** is formed not only on the movable plate **101** but also on the support **103**, and patterned to the shape of the elastic member **152**, as shown in FIG. 2B. After that, a metal film, the material of the driving coil **104**, is formed by means of sputtering, CVD, vacuum evaporation, plating, screen printing, or the like and then patterned by means of photolithographic techniques. Next, an insulating film **110** is formed on the metal film to cover the driving coil **104** and patterned to the shape of the elastic member **152**. The Si substrate is then etched using the first formed insulating film as a mask.

As clearly shown in this paragraph, there is no description or suggestion of etching an array of features, there is no description or suggestion of at least partially oxidizing an array of features, there is no description or suggestion to form a pad, and there is no description or suggestion of removing the pad. For at least these reasons, Claim 17 is patentable.

Dependent Claims 18-20 are patentable at least per the patentability of Claim 17 from which they depend. Moreover, Claims 18 and 20 are independently patentable. In particular, Claim 18 recites:

> 18. A method according to Claim 17 wherein the etching comprises etching an array of features in a silicon layer on an insulator layer on a substrate.

There is no description in the above passage that an array of features is etched anywhere, and there certainly no description or suggestion that the array of features is etched in the silicon layer on an insulator layer on a substrate. For example, the movable plate Si of Figure 14B does not appear to have anything etched therein. Accordingly, Claim 18 is independently patentable.

Finally, Claim 20 recites:

> 20. A method according to Claim 18 wherein the removing comprises:
> etching the substrate adjacent the pad;
> etching the insulating layer adjacent the pad; and

> etching the pad, from the insulating layer that was removed to the movable MEM structure.

There does not appear to be any description or suggestion in Minamoto Figure 14B or Column 7, lines 1-20 of etching the substrate adjacent the pad, because there is no pad. Similarly, there is no description or suggestion of etching the insulating layer adjacent the pad, because there is no pad. Finally, there is no description or suggestion of etching the pad, because there is no pad. Accordingly, Claim 20 is independently patentable.

Claims 9-10 and 16 Are Patentable Over Krusius et al. In View of Minamoto In Further View of Bhalla et al. In Further View of Little

Claims 9-10 and 16 are is patentable at least per the patentability of the independent claims from which they depend. Moreover, Claim 10 is independently patentable. Claim 10 recites:

> 10. A MEM mirror module according to Claim 9 wherein each of the MEM mirror substrates further comprises an underbump metallurgy between the frame and the solder bumps and wherein the underbump metallurgy and the metal layer on the MEM mirror substrate that is adjacent the base substrate both comprise a same metal. (Emphasis added.)

There is no description of underbump metallurgy in Little and, in particular, in Little Figure 6A, which does not even include solder bumps therein. Moreover, there is no description or suggestion in Little or any of the cited references of the above-underlined recitations of Claim 10. Accordingly, Claim 10 is independently patentable.

New Claims 21-31 Are Patentable

New Claims 21-29 have been filed to recite a particular application of embodiments of the present invention to optical cross-connect switches. As described in the present application, for example at Page 1, line 25-Page 2, line 2:

> Unfortunately, it may be difficult to fabricate large arrays of MEM devices with acceptable manufacturing yields. For example, in a 16 x 16 optical cross-connect switch, an array of 256 movable mirrors may be needed. It may be difficult to manufacture such an array with acceptable manufacturing yields.

Similarly, Page 3, lines 17-25 state:

> In some embodiments, each MEM mirror substrate **120** can include an array of four mirrors, in two rows and two columns. A 4 x 4 array of MEM mirror substrates **120** may be mounted on a base substrate **110** in four rows and four columns, to provide an array of 256 mirrors for a 16 x 16 optical cross-connect switch. This arrangement can allow higher manufacturing yields than may be obtained with a single array of 256 mirrors in a single MEM mirror substrate. It also will be understood that other numbers of mirrors and MEM mirror substrates may be used. Moreover, a single MEM mirror substrate **120** containing one or more mirrors also may be mounted on a base substrate **110**.

None of the cited references appear to describe or suggest optical cross-connect switches that include the recitations of Claims 21-29.

New Claim 30 recites:

> 30. A MEM mirror module according to Claim 7 wherein the second frame comprises monocrystalline silicon.

Assuming for the sake of argument that Minamoto describes a second frame, Minamoto clearly does not describe the second frame as comprising monocrystalline silicon. It would not be obvious to provide a MEM mirror module wherein the first frame and the second frame both are monocrystalline silicon. Accordingly, Claim 30 is independently patentable.

Finally, Claim 31 recites:

> 31. A MEM mirror according to Claim 8 wherein the metal layer on each of the opposing faces of the mirrors comprises a reflective metal layer on each of the opposing faces of the mirrors.

Assuming for the sake of argument that Minamoto describes a metal layer on each of the opposing faces of the mirrors, the Hall element and wiring layer of Minamoto may not be considered a reflective metal layer, as recited in Claim 31. Accordingly, Claim 31 is independently patentable.

Conclusion

Applicant again appreciates the thorough examination and detailed analysis in the Detailed Action. The cited references relate to movable microelectronic structures so that frames, hinges, substrates and the like may be present. However, Applicant has now shown that the claim recitations are not described or suggested in the cited references, even assuming that they are combined with hindsight. Accordingly,

Applicant respectfully requests withdrawal of the outstanding rejections and allowance of the present application.

Respectfully submitted,

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Attorney for Applicants

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20792
PATENT TRADEMARK OFFICE

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on February 4, 2003.

Susan E. Freedman
Date of Signature: February 4, 2003

Attorney Docket No. 9134-59

2873/##

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Robert L. Wood
Serial No.: 10/071,106
Filed: February 8, 2002
For: TILED MICROELECTROMECHANICAL DEVICE MODULES AND FABRICATION METHODS

Group Art Unit: 2873
Examiner: Joseph P. Martinez
Confirmation No.: 1445

February 4, 2003

Commissioner for Patents
Washington, DC 20231

Sir:

Transmitted herewith is an AMENDMENT in the above-identified patent application.

- ☐ Applicant claims small entity status. See 37 CFR §1.27.
- ☐ No additional fee is required.
- ☐ Other:

The fee has been calculated as shown below:

(COL. 1)		(COL. 2)	(COL. 3)	SMALL ENTITY		OTHER THAN A SMALL ENTITY	
	Claims Remaining After Amendment	Highest Number Previously Paid For	Present Extra	RATE	ADDIT. FEE	OR RATE	ADDIT. FEE
Total	* 31 -	** 20	= 11	x 09=	$	x 18=	$ 198.00
Indep	* 6 -	*** 4	= 2	x 42=	$	x 84=	$ 168.00
☐ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				+140=	$	+280=	$
				Total Add. Fee $		OR Total	$ 366.00

* If the entry in Col. 1 is less than the entry in Col. 2, write "0" in Col. 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, write "20" in this space.
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, write "3" in this space. The "Highest Number Previously Paid For" (Total or Independent) is the highest number found from the equivalent box in Col. 1 of a prior Amendment or the number of claims originally filed.

☒ Please charge my Deposit Account No. 50-0220 in the amount of $366.00.

☐ A check in the amount $_____ to cover the additional fee is enclosed.

☒ The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 50-0220.

- ☒ Any additional filing fees required under 37 C.F.R. § 1.16 for the presentation of extra claims.
- ☒ Any patent application processing fees under 37 C.F.R. § 1.17.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on February 4, 2003.

Susan E. Freedman
Date of Signature: February 4, 2003